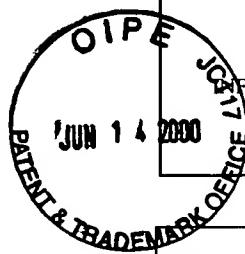


PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. RA001C10	SERIAL NUMBER 09/514,872
	APPLICANT(S) FARMWALD ET AL.	RECEIVED
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DA	4,330,852	May 18, 1982	Redwine et al.	—	—	
DA	4,703,418	Oct. 27, 1987	James	—	—	
DA	4,785,394	Nov. 15, 1988	Fischer	—	—	
DA	4,726,021	Feb. 16, 1988	Horiguchi et al.	—	—	
DA	4,870,562	Sept. 26, 1989	Kimoto et al.	—	—	

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EXAMINER INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
DA	S56-82961 ✓	July 7, 1981	Japan	—	—	YES
DA	S57-14922 ✓	Jan. 26, 1982	Japan	—	—	YES
DA	Sho 60-80193 ✓	May 8, 1983	Japan	—	—	YES
DA	Sho 60-55459 ✓	Mar. 30, 1985	Japan	—	—	YES
DA	S61-72350 ✓	April 14, 1986	Japan	—	—	YES
DA	S63-142445 ✗	June 14, 1988	Japan	—	—	YES
DA	B63-46864 ✓	Sept. 19, 1988	Japan	—	—	YES
DA	S64-29951 ✓	Jan. 31, 1989	Japan	—	—	YES

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

DA	Watanabe, T.; "Session XIX: High Density SRAMS"; IEEE International Solid State Circuits Conference pp. 266-267 (1987)
DA	Ohno, C.; "Self-Timed RAM: STRAM"; Fujitsu Sci. TechJ., 24, 4, pp 293-300 (Dec. 1988)
DA	"Fast Packet Bus for Microprocessor Systems with Caches", IBM Technical Disclosure Bulletin, pp.279-282 (Jan 1989)
DA	Gustavson, D. "Scalable Coherent Interface"; Invited Paper, COMPCON Spring '89, San Francisco, CA; IEEE, pp. 536-538 (Feb 27-Mar 3, 1989)
DA	James, D.; "Scalable I/O Architecture for Busses"; IEEE, pp. 539-544 (April 1989)

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EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
DA	4,205,373	May 27, 1980	Shah et al.	—	—	
DA	4,845,670	Jul. 4, 1989	Nishimoto et al.	—	—	
DA	4,509,142	Apr. 2, 1985	Childers	—	—	
AM	4,183,095	Jan. 8, 1980	Ward	—	—	
AM	4,685,088	Aug. 4, 1987	Ianucci	—	—	

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EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
DA	0 246 767	April 28, 1987	EPO	—	—	
DA	0 334 552	Mar. 16, 1989	EPO	—	—	
DA	0 276 871	Jan. 29, 1988	EPO	—	—	

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DA	European Search Report for EPO Patent Application No. 00 101 1832
DA	European Search Report for EPO Patent Application No. 89 30 2613
DA	Z. Amitai, "New System Architectures for DRAM Control and Error Correction", Monolithic Memories Inc., Electro/87 and Mini/Mico Northeast: Focusing on the OEM Conference Record, pp. 1132, 4/31-3, (April 1987)
DA	N. Siddique, "100-MHz DRAM Controller Sparks Multiprocessor Designs", Electronic Design, pp. 138-141, (Sept 1986)
DA	H. Kuriyama et al., "A 4-Mbit CMOS SRAM WITH 8-NS SERIAL ACCESS TIME", IEEE Symposium On VLSI Circuits Digest Of Technical Papers, pp. 51-52, (June 1990)
DA	J. Chun et al., "A 1.2ns GaAs 4K Read Only Memory", IEEE Gallium Arsenide Integrated Circuit Symposium Technical Digest, pp. 83-86, (Nov. 1988)
DA	A. Fielder et al., "A 3 NS 1K X 4 STATIC SELF-TIMED GaAs RAM", IEEE Gallium Arsenide Integrated Circuit Symposium Technical Digest, pp. 67-70, (Nov. 1988)
DA	JEDEC Standard No. 21C

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U.S. PATENT DOCUMENTS						
EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
<i>DA</i>	4,766,536	02/23/88	Wilson, Jr. et al.	—	—	
<i>DA</i>	4,998,262	03/05/91	Wiggers	—	—	
<i>DA</i>	4,747,079	03/24/88	Yamaguchi	—	—	
<i>DA</i>	4,649,511	03/10/87	Gdula	—	—	
<i>DA</i>	4,757,473	07/12/88	Kurihara et al.	—	—	
<i>DA</i>	4,792,926	12/20/88	Roberts	—	—	
<i>DA</i>	4,811,202	03/07/89	Schabowski	—	—	
<i>DA</i>	4,860,198	03/22/89	Takenaka	—	—	

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EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER <i>Glenn Aune</i>	DATE CONSIDERED <i>7/28/2000</i>
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U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		RECEIVED APR 17 2000	
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EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS
DA	4,754,433	06/28/88	Chin et al.	—	—
DA	5,023,488	06/11/91	Gunning	—	—
DA	4,920,486	04/24/90	Nielson	—	—
DA	4,719,602	01/12/88	Haq et al.	—	—
DA	4,263,650	04/21/81	Bennet et al.	—	—
DA	3,771,145	11/06/73	Wiener	—	—
DA	5,301,278	04/05/94	Bowater et al.	—	—
DA	5,175,835	12/29/92	Beighe et al.	—	—
DA	5,153,856	10/06/92	Takahashi	—	—
DA	5,051,889	09/24/91	Fung et al.	—	—
DA	5,034,917	07/23/91	Bland et al.	—	—
DA	3,691,534	09/12/72	Varadi et al	—	—
DA	3,969,706	07/13/76	Proebsting et al.	—	—

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EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO

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DA	M. Horowitz et al., "MIPS-X: A 20-MIPS Peak 32-bit Microprocessor with on-Chip Cache", IEEE Journal of Solid State Circuits, vol. 22 No. 5, pp. 790-799 (Oct. 1987)
DA	S Watanabe et. al., "An Experimental 16-Mbit CMOS DRAM Chip with a 100-MHz Serial READ/WRITE Mode", IEEE Journal of Solid State Circuits, vol. 24 No. 3, pp. 763-770 (June 1982)

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Glenn Aune	7/28/2000

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EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
<i>DA</i>	4,445,204	04/24/84	Nishiguchi	—	—	
<i>DA</i>	4,821,226	04/11/89	Christopher et al.	—	—	
<i>DA</i>	4,882,712	11/21/89	Ohno et. al.	—	—	
<i>DA</i>	4,951,251	08/21/90	Yamaguchi et al.	—	—	
<i>DA</i>	4,928,265	05/29/92	Beighe et al.	—	—	
<i>DA</i>	5,107,465	04/21/92	Fung et al.	—	—	
<i>DA</i>	4,206,833	04/27/93	Lee	—	—	
<i>DA</i>	4,953,128	08/28/90	Kawai et al.	—	—	
<i>DA</i>	5,140,688	08/18/92	White et al.	—	—	
<i>DA</i>	5,018,111	05/21/91	Madland	—	—	
<i>DA</i>	4,734,880	03/29/88	Collins	—	—	
<i>DA</i>	4,183,095	01/08/80	Ward	—	—	
<i>DA</i>	4,975,872	12/04/90	Zaiki	—	—	

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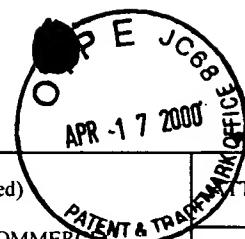
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO

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<i>DA</i>	T.L. Jeremiah et. al., "SYNCHRONOUS PACKET SWITCHING MEMORY AND I/O CHANNEL," IBM Tech. Disc. Bul. Vol. 24, No. 10, pp. 4986-4987 (Mar. 1982)
<i>DA</i>	L. R. Metzger, "A 16K CMOS PROM with Polysilicon Fusible Links", IEEE Journal of Solid State Circuits, vol. 18 No. 5, pp. 562-567 (Oct. 1983)

EXAMINER <i>Glen Anne</i>	DATE CONSIDERED <i>3/28/2000</i>
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PTO-1449 (Modified)		ATTY. DOCKET NO. RA001C10	SERIAL NUMBER 09/514,872	RECEIVED MAY 17 2000 GROUP 2700 2700
U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		APPLICANT(S) FARMWALD ET AL.		
INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>for F.C. and m.s.</i>		FILING DATE FEBRUARY 28, 2000	GROUP ART UNIT 2781	

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
JA	5,016,226	05/14/91	Hiwada et al.	—	—	
JA	5,109,498	04/28/92	Kamiya et al.	—	—	
JA	4,807,189	02/21/89	Pinkham et al.	—	—	
JA	4,092,665	05/30/78	Saran	—	—	
JA	4,799,199	01/17/89	Scales, III et al.	—	—	
JA	5,142,637	09/25/92	Harlin et al.	—	—	
JA	5,148,523	09/15/92	Harlin et al.	—	—	

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EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO

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JA	A. Yuen et. al., "A 32K ASIC Synchronous RAM Using a Two-Transistor Basic Cell", IEEE Journal of Solid State Circuits, vol. 24 No. 1, pp. 57-61 (Feb. 1989)
JA	D.T. Wong et. al., "An 11-ns 8Kx18 CMOS Static RAM with 0.5-μm Devices", IEEE Journal of Solid State Circuits, vol. 23 No. 5, pp. 1095-1103 (Oct. 1988)
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JA	F. Towler et. al., "A 128k 6.5ns Access/ 5ns Cycle CMOS ECL Static RAM", 1989 IEEE International Solid State Circuits Conference, (Feb. 1989)

EXAMINER <i>Glenn Anne</i>	DATE CONSIDERED <i>7/28/2000</i>
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Sheet 5 of 6

PTO-1449 (Modified)		ATTY. DOCKET NO. RA001C10	SERIAL NUMBER 09/514,872
U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		RECEIVED MAY 17 2000 APPLICANT(S) FARMWALD ET AL.	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		FILING DATE FEBRUARY 28, 2000	GROUP ART UNIT 2781 GROUP 2700

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EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
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JA	4,954,987	09/04/90	Auvinen et al.	—	—	
JA	4,675,850	06/23/87	Kumanoya et al.	—	—	
JA	4,788,667	11/29/88	Nakano et al.	—	—	
JA	4,945,516	07/31/90	Kashiyama	—	—	
JA	4,937,734	06/26/90	Bechtolsheim	—	—	
JA	4,845,664	07/04/89	Aichelmann, Jr. et al.	—	—	
JA	4,920,483	04/24/90	Pogue et al.	—	—	
JA	4,680,738	07/14/87	Tam	—	—	

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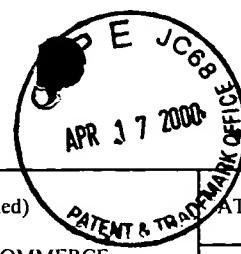
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JA	H. L. Kalter et al. "A 50-ns 16Mb DRAM with a 10-ns Data Rate and On-Chip ECC" IEEE Journal of Solid State Circuits, vol. 25 No. 5, pp. 1118-1128 (Oct 1990)
JA	D. Wendell et. al. "A 3.5ns, 2Kx9 Self Timed SRAM", 1990 IEEE Symposium on VLSI Circuits (Feb 1990)
JA	M. Bazes et. al. "A Programmable NMOS DRAM Controller for Microcomputer Systems with Dual-Port Memory and Error Checking and Correction", IEEE Journal of Solid State Circuits, vol. 18 No. 2, pp. 164-172 (Apr. 1983)
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DA	5,390,149	02/14/95	Vogley et al.	—	—	
MM	4,570,220	02/11/86	Tetrick et al.	—	—	
MM	5,083,296	01/21/92	Hara et al.	—	—	
MM	5,077,693	12/31/91	Hardee et al.	—	—	
MM	4,916,670	04/10/90	Suzuki et al.	—	—	
MM	4,247,817	1/27/81	Heller	—	—	
MM	5,301,278	04/05/94	Bowater et al.	—	—	
MM	4,970,418	11/13/90	Masterson	—	—	
MM	5,361,277	11/01/94	Grover	—	—	
MM	4,519,034	05/21/85	Smith et al.	—	—	
MM	4,315,308	02/09/82	Jackson	—	—	
MM	3,821,715	06/28/74	Hoff, Jr et al.	—	—	

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